WHAT IS CLAIMED IS:

1. A method of detecting a phase difference between a recovered clock and a received serial bitstream, the recovered clock having at least first and second clock phases, the method comprising:

generating an integration window defined at least in part by the first clock phase and the second clock phase;

sampling at least portions of two bitstream bits and a transition region between the two bitstream bits; and

integrating within the integration window over at least the portions of two bitstream bits and the transition region between the two bits by changing a charge of at least a first capacitor so that the magnitude of the charge is related to a phase relationship between the bitstream and the recovered clock, wherein the capacitor charge is used to synchronize the recovered clock with the serial bitstream.

2. The method as defined in Claim 1, wherein both the sampling and integration are performed using the at least first capacitor.

3. The method as defined in Claim 1, wherein the first capacitor is used to integrate bitstream bits having a first logic value and a second capacitor is used to integrate bitstream bits having a second logic value.

4. The method as defined in Claim 1, wherein the magnitude of the charge is related to the amount of time within the integration window the portions of two bitstream bits are at a first logic level.

5. The method as defined in Claim 1, wherein the at least first capacitor is discharged during integration.

6. The method as defined in Claim 1, wherein the bitstream is received as a differential signal.

7. The method as defined in Claim 1, wherein the capacitor charge value changes only when the two bitstream bits have corresponding different logic levels.

8. A method of determining phase differences between an encoded clock and a generated clock, wherein the encoded clock is derived from an encoded data stream, the method comprising:

receiving the encoded data stream;

initiating an integration process at least partly in response to a first state of the generated clock;

integrating over a portion of a first data stream bit, a portion of an adjacent second data stream bit, and a transition region between the first data stream bit and the second data stream bit, to generate an integration value; and

generating a phase difference signal related to a phase difference between the encoded clock and the generated clock based at least in part on the integration value.

9. The method as defined in Claim 8, wherein the integration is performed using a first capacitor and a second capacitor coupled to the data stream, wherein the first capacitor is used to sequentially integrate at least portions of first data stream bits having a first logic level and the second capacitor is used to sequentially integrate at least portions of first data stream bits having a second logic level.

10. The method as defined in Claim 8, wherein the integration is performed over a fixed window period.

11. The method as defined in Claim 8, wherein the phase difference signal is used to synchronize the generated clock with the encoded clock.

12. The method as defined in Claim 8, wherein the generated clock is generated using a voltage controlled oscillator.

13. The method as defined in Claim 8, wherein the first data stream bit has a different logical value than the second data stream bit.

14. The method as defined in Claim 8, further comprising demultiplexing the received encoded data stream prior to the integration process.

15. A system configured to determine a phase difference between a first clock and a second clock, wherein the second clock is encoded in a bitstream, the system comprising:

a voltage controlled oscillator clock generation circuit configured to generate the first clock;

an integration trigger circuit configured to generate an integration initiation signal in response to a level transition of the first clock;

an integration circuit coupled to the integration trigger circuit, the integration circuit configured to sample and integrate over at least portions of two adjacent bitstream bits, including a transition region between the two adjacent bits, and to generate an integration value; and

a phase difference circuit coupled to the integration circuit, the phase difference circuit configured to determine the phase difference between the first clock and the second clock based at least in part on the integration value.

16. The system as defined in Claim 15, wherein the integration circuit includes a first capacitor used to integrate bits corresponding to a first logic level and a second capacitor used to integrate bits corresponding to a second logic level.

17. The system as defined in Claim 16, wherein the phase difference circuit determines the phase difference at least in part by a comparison of a charge-related value of the first capacitor with a charge-related value of the second capacitor.

18. The system as defined in Claim 15, wherein the voltage controlled oscillator clock generation circuit includes a phase demultiplexer circuit configured to generate a plurality of clocks that includes the first clock, the plurality of clocks having corresponding different phases.

19. The system as defined in Claim 15, wherein the integration trigger circuit is further configured to halt integration in response a level transition of a third clock, the third clock generated by the voltage controlled oscillator clock generation circuit.

20. The system as defined in Claim 15, wherein the phase difference is used to synchronize the first clock with the second clock.

21. A network interface circuit, comprising:

a first interface port configured to receive a serial bitstream from a network;

a receiver clock generator configured to generate a receiver clock, including a first clock signal having a first clock phase and a second clock signal having a second clock phase;

an integration window generator circuit coupled to the first clock signal and the second clock signal, wherein the integration window generator circuit generates an integration window defined at least in part by the first clock signal and the second clock signal; and

a bitstream integrator circuit configured to integrate within a period defined by the integration window over at least portions of two serial bitstream bits and a transition region between the two bits by changing a charge of at least a first capacitor so that the magnitude of the capacitor charge is related to a phase relationship between the serial bitstream and the receiver clock, wherein the magnitude of the capacitor charge is used to synchronize the receiver clock with the serial bitstream.

22. The network interface circuit as defined in Claim 21, wherein the bitstream integrator circuit further comprises a second capacitor configured to integrate bits having a first logic level, and wherein the first capacitor is configured to integrate bits having a second logic level.

23. The network interface circuit as defined in Claim 22, wherein a difference in capacitor charge magnitude of the first capacitor and the second capacitor is related to the phase relationship between the serial bitstream and the receiver clock.

24. The network interface circuit as defined in Claim 21, further comprising a serial bitstream demultiplexer circuit positioned between the first interface port and the bitstream integrator circuit, wherein the serial bitstream demultiplexer circuit demultiplexes the serial bitstream in response to at least the first clock signal and the second clock signal, the serial bitstream demultiplexer circuit further configured to provide at least a portion of the demultiplexed serial bitstream to the bitstream integrator circuit.

25. A networked system including a plurality of computer systems and local area networks (LANs), comprising:

a first plurality of computer systems;

a first LAN coupled to the first plurality of computer systems;

a second plurality of computer systems; and

a second LAN coupled to the second plurality of computer systems;

an optical network coupled to the first LAN using a first interface circuit and to the second LAN by a second interface circuit, wherein each of the first interface circuit and the second interface circuit include:

a transceiver circuit configured coupled to at least one LAN and to the optical network, the transceiver circuit further configured to receive a data bitstream from the optical network, the transceiver circuit including:

a clock generation circuit configured to generate at least a first clock signal;

an integration window generator circuit coupled to the first clock signal, wherein the integration window generator circuit generates an integration window defined at least in part by the first clock signal;

an integration circuit configured to integrate over at least portions of two adjacent bits from the data bitstream, and to generate an integration value; and

a phase difference circuit configured to determine the phase difference between the first clock and the data stream based at least in part on the integration value, wherein the phase difference is used to synchronize the first clock with the data bitstream.

26. The networked system as defined in Claim 25, wherein the integration circuit includes a first storage device used to integrate bits corresponding to a first logic level, and a second storage device used to integrate bits corresponding to a second logic level.

27. The networked system as defined in Claim 25, wherein the first and the second LANs are Ethernet networks and the optical network is a SONET network.